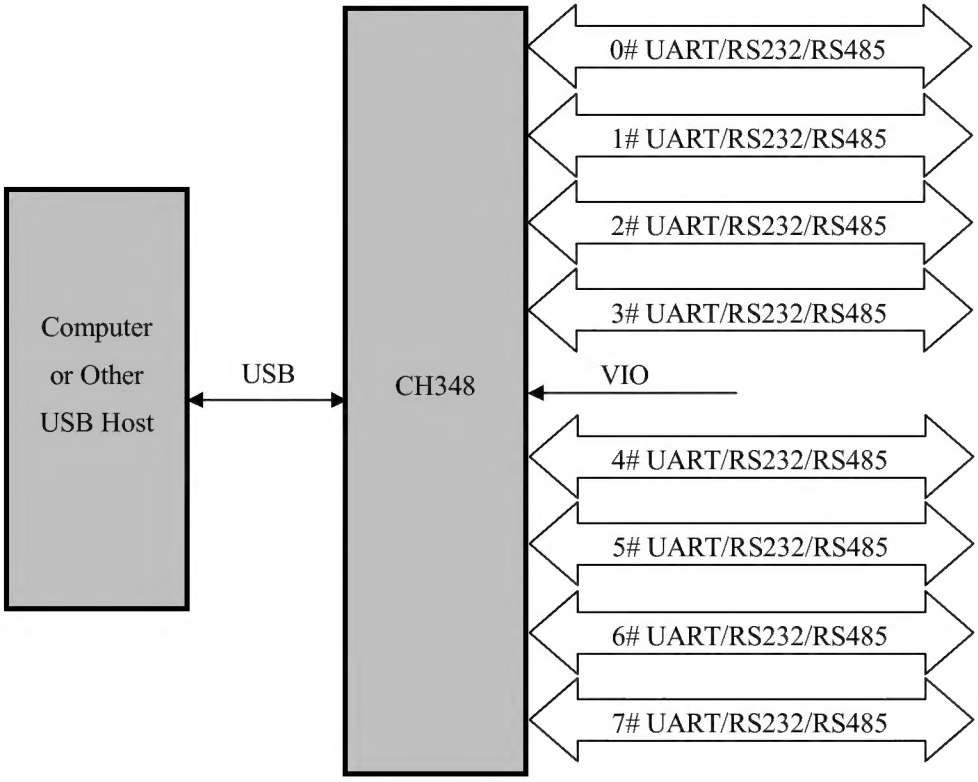
USB to Octal Serial Ports Chip CH348

Datasheet
Version: 1C
http://wch.cn

1. Introduction

CH348 is a high-speed USB bus converter chip, which converts USB to octal serial ports UART0/1/2/3/4/5/6/7, and used to expand serial ports for computer or upgrade directly from normal serial device or MCU to USB bus.



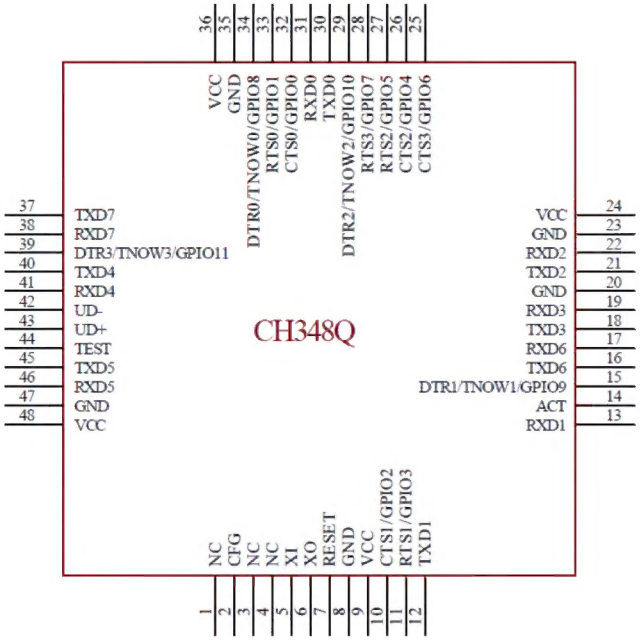
2. Features

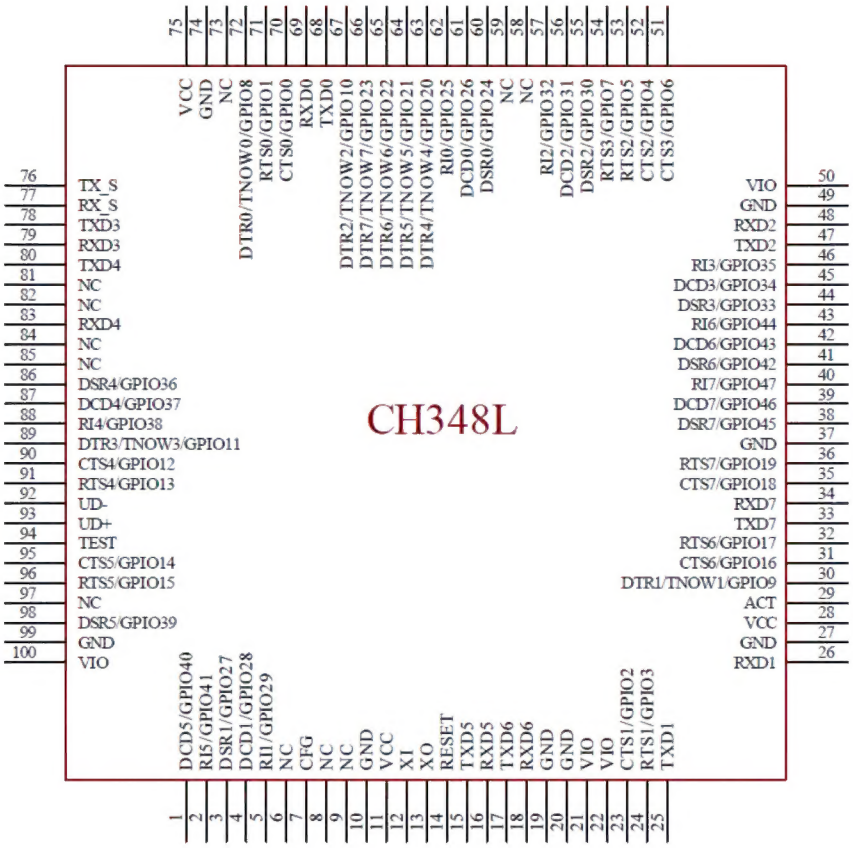
- 480Mbps high-speed USB device interface, peripheral components only need crystal oscillator and capacitors.
- Built-in firmware, emulate standard UART interface, used to upgrade the original serial peripheral or expand additional UART via USB.
- Original serial applications are totally compatible without any modification in Windows operating systems.
- Hardware full duplex UART interface, integrated independent transmit-receive buffer, supports communication baud rate varies from 1200bps to 6Mbps.
- UART supports 8 data bits, supports odd, even, and none parity, supports 1 or 2 stop bits.
- Integrated the 2048-byte RX FIFO and 1024-byte TX FIFO for each UART.
- Supports common MODEM signals RTS, DTR, DCD, RI, DSR and CTS.
- Supports CTS and RTS hardware automatic flow control.
- Supports half-duplex, provides sending status TNOW, used for controlling RS485 to

transmit-receive switch.

- Supports up to 48-channel GPIO input and output function.
- Supports RS232/RS485/RS422 interface, through external voltage conversion chip.
- UART I/O of CH348L power supply independently, supports 3.3V, 2.5V, 1.8V power supply voltages.
- Built-in EEPROM used to configure the chip of VID, PID, maximum current value, vendor and product information string, etc.
- Supports only 3.3V power supply.
- RoHS compliant LQFP48 and LQFP100 lead-free package.

3. Packages





Package	Body size	Lead pitch		Description	Part No.
LQFP48	7*7mm	0.5mm	19.7mil	Standard LQFP48 pin patch	CH348Q
LQFP100	14*14mm	0.5mm	19.7mil	Standard LQFP100 pin patch	CH348L

Note: The USB transceiver of CH348 is designed according to the built-in design of USB2.0, and it is recommended that no external resistor is in series with UD+ and UD- pins.

4. Pin definitions

Pin No.		Pin Name	Pin Type	Pin Description
LQFP100	LQFP48			
11, 28, 75	9, 24, 36, 48	VCC	POWER	Power supply voltage input, requires an external decoupling capacitor
21, 22, 50, 100		VIO	POWER	I/O Power supply voltage input, requires an external decoupling capacitor
10, 19, 20, 27, 37, 49, 74, 99	8, 20, 23, 35, 47	GND	POWER	Ground, connected to ground of USB bus directly
14	7	RESET	IN	Input of external reset, active low, built-in pull-up resistor
93	43	UD+	USB signal	Connect to USB D+ Signal directly, do not series resistors
92	42	UD-	USB signal	Connect to USB D- Signal directly, do not series resistors
12	5	XI	IN	Input of crystal oscillator,
13	6	XO	OUT	Inverted output of crystal oscillator
68	30	TXD0	OUT	Transmit asynchronous data output of UART0, high when idle
69	31	RXD0	IN (FT)	Receive asynchronous data input of UART0, built-in pull-up resistor
25	12	TXD1	OUT	Transmit asynchronous data output of UART1, high when idle
26	13	RXD1	IN	Receive asynchronous data input of UART1, built-in pull-up resistor

47	21	TXD2	OUT	Transmit asynchronous data output of UART2, high when idle
48	22	RXD2	IN (FT)	Receive asynchronous data input of UART2, built-in pull-up resistor
78	18	TXD3	OUT	Transmit asynchronous data output of UART3, high when idle
79	19	RXD3	IN	Receive asynchronous data input of UART3, built-in pull-up resistor
80	40	TXD4	OUT	Transmit asynchronous data output of UART4, high when idle
83	41	RXD4	IN (FT)	Receive asynchronous data input of UART4, built-in pull-up resistor
15	45	TXD5	OUT	Transmit asynchronous data output of UART5, high when idle
16	46	RXD5	IN	Receive asynchronous data input of UART5, built-in pull-up resistor
17	16	TXD6	OUT	Transmit asynchronous data output of UART6, high when idle
18	17	RXD6	IN	Receive asynchronous data input of UART6, built-in pull-up resistor
33	37	TXD7	OUT	Transmit asynchronous data output of UART7, high when idle
34	38	RXD7	IN (FT)	Receive asynchronous data input of UART7, built-in pull-up resistor
72	34	DTR0/ TNOW0/ GPIO8	OUT IN (FT)	MODEM output signal of UART0, data terminal ready, active low; RS485 transmit and receive control pin of UART0; General GPIO8, used for IO input or output
30	15	DTR1/ TNOW1/ GPIO9	OUT/IN	MODEM output signal of UART1, data terminal ready, active low; RS485 transmit and receive control pin of UART1; General GPIO9, used for IO input or output

67	29	DTR2/ TNOW2/ GPIO10	OUT IN (FT)	MODEM output signal of UART2, data terminal ready, active low; RS485 transmit and receive control pin of UART2,; General GPIO10, used for IO input or output
89	39	DTR3/ TNOW3/ GPIO11	OUT IN (FT)	MODEM output signal of UART3, data terminal ready, active low,; RS485 transmit and receive control pin of UART3; general GPIO11, used for IO input or output
63		DTR4/ TNOW4/ GPIO20	OUT IN (FT)	MODEM output signal of UART4, data terminal ready, active low; RS485 transmit and receive control pin of UART4; General GPIO20, used for IO input or output
64		DTR5/ TNOW5/ GPIO21	OUT IN (FT)	MODEM output signal of UART5, data terminal ready, active low; RS485 transmit and receive control pin of UART5; General GPIO21, used for IO input or output
65		DTR6/ TNOW6/ GPIO22	OUT IN (FT)	MODEM output signal of UART6, data terminal ready, active low; RS485 transmit and receive control pin of UART6; General GPIO22, used for IO input or output
66		DTR7/ TNOW7/ GPIO23	OUT IN (FT)	MODEM output signal of UART7, data terminal ready, active low; RS485 transmit and receive control pin of UART7; General GPIO23, used for IO input or output
70	32	CTS0/ GPIO0	IN (FT)	MODEM input signal of UART0, clear to send, active low, general GPIO0, used for IO input or output
71	33	RTS0/ GPIO1	OUT	MODEM output signal of UART0, request to send, active low, general GPIO1, used for IO input or output, if RST0 detects that an external pull-down resistor is connected during power-on, disable internal EEPROM configuration parameter, enable chip default parameter
23	10	CTS1/ GPIO2	IN	MODEM input signal of UART1, clear to send, active low, general GPIO2, used for IO input or output
24	11	RTS1/ GPIO3	OUT	MODEM output signal of UART1, request to send, active low, general GPIO3, used for IO input or output

52	26	CTS2/ GPIO4	IN (FT)	MODEM input signal of UART2, clear to send, active low, general GPIO4, used for IO input or output
53	27	RTS2/ GPIO5	OUT	MODEM output signal of UART2, request to send, active low, general GPIO5, used for IO input or output
51	25	CTS3/ GPIO6	IN (FT)	MODEM input signal of UART3, clear to send, active low, general GPIO6, used for IO input or output
54	28	RTS3/ GPIO7	OUT	MODEM output signal of UART3, request to send, active low, general GPIO7, used for IO input or output
90		CTS4/ GPIO12	IN (FT)	MODEM input signal of UART4, clear to send, active low, general GPIO12, used for IO input or output
91		RTS4/ GPIO13	OUT	MODEM output signal of UART4, request to send, active low, general GPIO13, used for IO input or output
95		CTS5/ GPIO14	IN (FT)	MODEM input signal of UART5, clear to send, active low, general GPIO14, used for IO input or output
96		RTS5/ GPIO15	OUT	MODEM output signal of UART5, request to send, active low, general GPIO15, used for IO input or output
31		CTS6/ GPIO16	IN	MODEM input signal of UART6, clear to send, active low, general GPIO16, used for IO input or output
32		RTS6/ GPIO17	OUT	MODEM output signal of UART6, request to send, active low, general GPIO17, used for IO input or output
35		CTS7/ GPIO18	IN	MODEM input signal of UART7, clear to send, active low, general GPIO18, used for IO input or output
36		RTS7/ GPIO19	OUT	MODEM output signal of UART7, request to send, active low, general GPIO19, used for IO input or output
60		DSR0/ GPIO24	IN (FT)	MODEM input signal of UART0, data set ready, active low, general GPIO24, used for IO input or output
62		RI0/ GPIO25	IN (FT)	MODEM input signal of UART0, ring indicator, active low, general GPIO25, used for IO input or output
61		DCD0/ GPIO26	IN (FT)	MODEM input signal of UART0, data carrier detect, active low, general GPIO26, used for IO input or output
3		DSR1/ GPIO27	IN (FT)	MODEM input signal of UART1, data set ready, active low, general GPIO27, used for IO input or output

5		RI1/ GPIO29	IN (FT)	MODEM input signal of UART1, ring indicator, active low, general GPIO29, used for IO input or output
4		DCD1/ GPIO28	IN (FT)	MODEM input signal of UART1, data carrier detect, active low, general GPIO28, used for IO input or output
55		DSR2/ GPIO30	IN (FT)	MODEM input signal of UART2, data send ready, active low, general GPIO30, used for IO input or output
57		RI2/ GPIO32	IN (FT)	MODEM input signal of UART2, ring indicator, active low, general GPIO32, used for IO input or output
56		DCD2/ GPIO31	IN (FT)	MODEM input signal of UART2, data carrier detect, active low, general GPIO31, used for IO input or output
44		DSR3/ GPIO33	IN (FT)	MODEM input signal of UART3, data set ready, active low, general GPIO33, used for IO input or output
46		RI3/ GPIO35	IN (FT)	MODEM input signal of UART3, ring indicator, active low, general GPIO35, used for IO input or output
45		DCD3/ GPIO34	IN (FT)	MODEM input signal of UART3, data carrier detect, active low, general GPIO34, used for IO input or output
86		DSR4/ GPIO36	IN (FT)	MODEM input signal of UART4, data set ready, active low, general GPIO36, used for IO input or output
88		RI4/ GPIO38	IN (FT)	MODEM input signal of UART4, ring indicator, active low, general GPIO38, used for IO input or output
87		DCD4/ GPIO37	IN (FT)	MODEM input signal of UART4, data carrier detect, active low, general GPIO37, used for IO input or output
98		DSR5/ GPIO39	IN (FT)	MODEM input signal of UART5, data set ready, active low, general GPIO39, used for IO input or output
2		RI5/ GPIO41	IN (FT)	MODEM input signal of UART5, ring indicator, active low, general GPIO41, used for IO input or output
1		DCD5/ GPIO40	IN (FT)	MODEM input signal of UART5, data carrier detect, active low, general GPIO40, used for IO input or output
41		DSR6/ GPIO42	IN (FT)	MODEM input signal of UART6, data set ready, active low, general GPIO42, used for IO input or output
43		RI6/ GPIO44	IN (FT)	MODEM input signal of UART6, ring indicator, active low, general GPIO44, used for IO input or output

42		DCD6/ GPIO43	IN (FT)	MODEM input signal of UART6, data carrier detect, active low, general GPIO43, used for IO input or output
38		DSR7/ GPIO45	IN (FT)	MODEM input signal of UART7, data set ready, active low, general GPIO45, used for IO input or output
40		RI7/ GPIO47	IN (FT)	MODEM input signal of UART7, ring indicator, active low, general GPIO47, used for IO input or output
39		DCD7/ GPIO46	IN (FT)	MODEM input signal of UART7, data carrier detect, active low, general GPIO46, used for IO input or output
29	14	ACT	OUT	USB configuration completed status output, active low
94	44	TEST	IN	Internal test pin, recommended that connects to ground with an pull-down resistor (usually value is 4.7kΩ) or connects to ground directly
7	2	CFG	IN	TNOW and DTR function configuration pin, optional unified configuration or independent configuration. Unified configuration: During power-on, if the CFG pin is at a high level or not connected, all DTRx/ TNOWx pins are configured to function as TNOW. CFG pin is low, all DTRx/ TNOWx pins are configured for DTR function. Independent configuration: During power-on, the CFG pin should be low level, for the UART which need to be configured as TNOW function need to connect a pull-down resistance (such as 4.7KΩ) to the DTRx/ TNOWx pin of the corresponding UART to the ground separately. If the pin is not connected to the pull-down resistance, it will configured as DTR function.
76		TX_S	OUT	UART data transmitting status output
77		RX_S	OUT	UART data receiving status output
6, 8, 9, 58, 59, 73, 81, 82, 84, 85, 97	1, 3, 4	NC	None	No connection, do not connect

Note1: The power supply of RTS0, CTS0, DTR4, DTR5, DTR6 and DTR7 pins of CH348L come from VCC, these pins are 3.3V signal level. The power supply of other UARTs and MODEM signal pins come from VIO, which are 3.3V/2.5V/1.8V matching VIO signal level.

Note2: FT means the pin can tolerate 5V voltage when used as input.

5. Function descriptions

5.1. General description

CH348L has 2 power supplies VCC and VIO, CH348Q has only VCC. VCC is the input of main power supply, VIO is the input of I/O power supply, VCC supports 3.3V power supply voltage, VIO supports 1.8V, 2.5V, 3.3V power supply voltages. The power pins VCC and VIO should be respectively connected to an external power decoupling capacitor of about 0.1uF. The UD+ and UD- pins should be connected directly to the USB bus, with ESD protection devices connected in parallel if required.

CH348 has a built-in power-on reset circuit. When the chip is operating, it needs to provide an external 8MHz clock signal to the XI pin. The clock signal can be generated by the built-in inverter of CH348 through crystal frequency stabilization oscillation. The peripheral circuit needs to connect an 8MHz crystal between the XI and XO pins, and the both pins connect to the ground with an oscillation capacitor of about 20pF.

CH348 has built-in all the peripheral circuits required by the USB bus, including the embedded USB controller and USB-PHY, the series matching resistor of the USB signal line, and the 1.5K pull-up resistor required for the device.

5.2. UART description

CH348 provides octal serial ports UART0~7, each UART includes TXD and RXD pin, full-featured package contains all MODEM pins, it can realize 3-line UART, 5-line or 9-line UART communication.

In UART mode, CH348 contains: data transfer pins, MODEM interface signal pins and assistant pins.

Data transfer pins contain: 8 groups of TXD0~7 and RXD0~7, RXDx is high when UART reception is idle. TXDx is high when UART transmission is idle.

MODEM interface signal pins and RS485 transmit and receive control pins:

CH348Q contains 4 groups pin of CTS0~3, RTS0~3 and 4 groups of DTR0-3(TNOW0~3).
CH348L contains 8 groups pin of CTS0~7, RTS0~7, DSR0~7, DCD0~7, RI0~7 and DTR0~7(TNOW0~7).

Assistant pins contain: ACT, TX_S, RX_S and CFG, etc. The ACT is the output pin of USB device configuration completed status. The default outputs high level during power-on and outputs low level after the USB host performs USB configuration on CH348. TX_S is the output pin of the chip's UART sending data status. When any serial port is sending data, TX_S outputs a pulse level with a period of 200mS. RX_S is the output pin of the chip's UART receiving data status. When any serial port is receiving data, RX_S outputs a pulse level with a period of 200mS. CFG is TNOW and DTR function configuration pin. The chip detects the level status of this pin when power-on. If it is not connected or inputs high level, TNOW function will be enabled; inputs low level will enable DTR function.

TNOW and DTR function configuration pin, optional unified configuration or independent configuration.

Unified configuration: During power-on, if the CFG pin is at a high level or not connected, all DTRx/TNOWx pins are configured to function as TNOW. CFG pin is low, all DTRx/TNOWx pins are configured for DTR function.

Independent configuration: During power-on, the CFG pin is connected to a low level and needs to be

configured as a UART for the TNOW function. Then, connect a pull-down resistance (such as 4.7KΩ) to the DTRx/TNOWx pin of the corresponding UART to the ground. If the pin is not connected to the pull-down resistance, configure the DTR function.

Each UART of CH348 has built-in independent transmit-receive buffer and supports simplex, half-duplex and full-duplex asynchronous serial communication.

The serial data of CH348 contains a low-level start bit, 8 data bits and 1/2 high-level stop bits, supports none/odd/even parity. The common communication baud rate: 1200, 1800, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 33600, 38400, 56000, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5M, 2M, 3M, 4M, 5M, 6M, etc.

The eight UARTs of CH348 all support CTSx and RTSx hardware automatic flow control, which can be enabled or disabled (default) through the VCP vendor driver. If enabled, UART only will continue to send the next data when CTSx input is valid (active low), otherwise the UART transmission will be stopped; UART will automatically set RTSx to be valid (active low) when the receiving buffer is empty, it will automatically invalidate RTSx until the data in the receiving buffer is nearly full, and RTSx will be valid again when the buffer is empty. While using hardware automatic rate control, CTSx of CH348 should connect to RTSx of the counterpart, and RTSx of CH348 should connect to CTSx of the counterpart.

The allowable baud rate error of CH348's UART receiving signal is less than 2%, the baud rate error of UART transmitting signal is less than 1%.

In the Windows OS, after installing high-speed VCP vendor driver, it can emulate standard UART, so the mostly original serial applications are totally compatible, without any modification.

CH348 can support up to 48-channel GPIO input and output function.

CH348 can be used to upgrade the original serial port peripheral devices, or expand extra serial port for computers via USB bus. Through external level shifting chip provides RS232, RS485, RS422 and other interfaces can be further.

5.3. Parameter configuration

In larger batch applications, the vendor VID and product identification PID of CH348 and product information can be customized.

In less batch applications, it can use the built-in EEPROM for parameter configuration. After user installs VCP vendor driver, through configuration tool CH34xSerCfg.exe provided by chip manufacturer, it can be flexibly configured the vendor VID, product identification PID, maximum current value, BCD version number, manufacture information and product information string descriptor, etc.

6. Parameters

6.1. Absolute maximum ratings

(Operating in critical ratings or exceeding the absolute maximum ratings may cause chip to not work or even be damaged)

Name	Parameter Description	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-40	125	℃

VCC	Supply voltage(VCC connects to power, GND connects to ground)	-0.3	4.0	V
VIO	I/O supply voltage	-0.3	4.0	V
VUSB	USB signal voltage	-0.5	3.8	V
VIO5V	5V tolerant on the UART pins	-0.5	5.6	V
VUART	UART and others voltage	-0.5	VCC+0.3	V

6.2. Electrical characteristics

(Test conditions: TA=25℃, VCC =3.3V, exclude USB pin)

Symbol	Parameter Description	Min.	Typ.	Max.	Unit
VCC	Supply voltage(VCC power supply, GND connects to ground)	3.0	3.3	3.6	V
VIO	UART I/O supply voltage	1.7	3.3	3.6	V
ICC	Operating supply current	28	40	55	mA
ISLP	Supply current(USB suspend)	180	260	360	uA
VIL	Input low voltage	0		0.8	V
VIH	Input high voltage	2.0		VCC	V
VIH5	Tolerate high level input voltage for 5V pins	2.0		5.0	V
VOL	Output low voltage, single pin 8mA sunk current			0.4	V
VOH	Output high voltage, single pin outputs 8mA current	VCC-0.4			V
RPU	Built-in pull-up equivalent resistance	30	40	60	KΩ
VPOR	Threshold voltage for power on / power off reset	1.9	2.2	2.5	V
VESD	ESD electrostatic discharge voltage (mannequin, non-contact)	4			KV

6.3. Timing parameters

(Test conditions: TA=25℃, VCC= 3.3V)

Symbol	Parameter Description	Min.	Typ.	Max.	Unit
TRSTD	Reset delay after power-on or external reset input	15	30	40	mS
TSUSP	Detect USB automatic suspend time	3	5	9	mS
TWAKE	Wake-up completion time after chip sleep	0.3	0.5	4	mS

7. Application

7.1. USB to 8-channel TTL UART

The below image is the USB to 8-Channel TTL UART convert by CH348. The signal line in the image can only be connected to RXDx, TXDx and public ground. CTSx, RTSx, TNOWx can be selected as needed, and all can be not connected when not needed.

P1 is USB port, USB bus contains a pair of 5V power lines and a pair of data signal lines. Usually, the color of +5V power line is red, the black is ground. D+ signal line is green and the D- is white. The supply current provided by USB bus can up to 500mA.

P2, P3, P4, P5, P6, P7, P8 and P9 are the TTL connection pins of each serial port, including: VCC, GND, RXDx, TXDx, RTSx, CTSx, and DTRx/TNOWx, etc. Level conversion chip can be added to realize signal conversion (Must support high baud rate) from TTL to RS232, RS485 and RS422, etc. When more MODEM signals are needed, CH348L can be used instead.

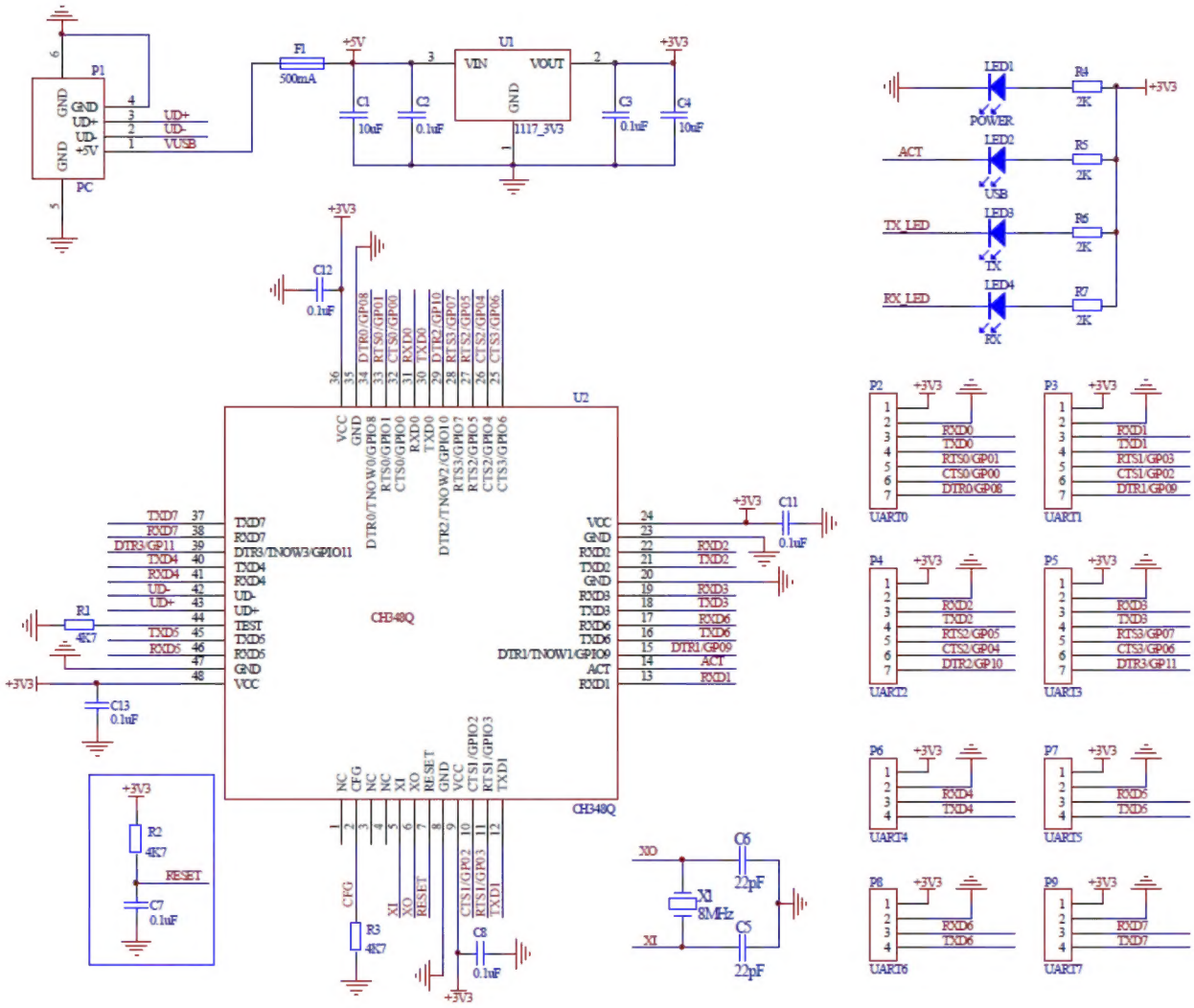
VCC pin of CH348 inputs 3.3V power supply voltage, each power pin should be connected to a power decoupling capacitor with a capacity of about 0.1uF. In the image, C8, C10, C12 and C13 are power decoupling capacitors. CH348L with VIO power supply pin can be used instead when it needs to support signal levels such as 2.5V or 1.8V.

Crystal X1, capacitors C5 and C6 are used in the clock oscillation circuit of CH348. The frequency of X1 is 8MHz±0.4‰, C5 and C6 are monolithic or high-frequency ceramic capacitors with a capacity of about 22pF, and R2 and C7 are optional components.

It is recommended to add ESD protection device for USB signal line. The parasitic capacitance of ESD chip should be less than 2pF, such as ch412k.

It is recommended that the serial port peripherals and CH348 use the same power supply. Otherwise, the I/O pin reverse current when the serial port peripherals are powered separately must be considered.

When designing the PCB, pay attention to: decoupling capacitor C8,C11,C12 and C13 get as close to the connected power pin of CH348 as possible. The D+ and D- signal lines of the USB port are routed close to parallel according to the high-speed USB specification to ensure the characteristic impedance, and providing ground or copper on both sides to reduce signal interference from the outside.


P1
PC
GND
UD+
UD-
+5V
VUSB
F1
500mA
+5V
+3V3
U1
VIN
VOUT
GND
1117_3V3
C1
10uF
C2
0.1uF
C3
0.1uF
C4
10uF
LED1
POWER
LED2
ACT
USB
LED3
TX_LED
TX
LED4
RX_LED
RX
R4
R5
R6
R7
2K
C12
0.1uF
U2
CH348Q
VCC
GND
DTR0/TNOW0/GPIO8
RTS0/GPIO1
CTS0/GPIO0
RXD0
TXD0
DTR2/TNOW2/GPIO10
RTS3/GPIO7
RTS2/GPIO5
CTS2/GPIO4
CTS3/GPIO6
TXD7
RXD7
DTR3/GP11
TXD4
RXD4
UD-
UD+
TEST
TXD5
RXD5
DTR3/TNOW3/GPIO11
R1
4K7
C13
0.1uF
RXD2
TXD2
RXD3
TXD3
RXD6
TXD6
DTR1/TNOW1/GPIO9
ACT
RXD1
C11
0.1uF
NC
CFG
RESET
CTS1/GPIO2
RTS1/GPIO3
TXD1
R2
4K7
C7
0.1uF
R3
4K7
C8
0.1uF
XO
XI
X1
8MHz
C6
22pF
C5
22pF
P2
P3
P4
P5
P6
P7
P8
P9
UART0
UART1
UART2
UART3
UART4
UART5
UART6
UART7